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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/619,144	07/15/2003	Aphrodite Chen	COR 128	6077

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EXAMINER	
JAIN, RAJ K	
ART UNIT	PAPER NUMBER
2416	
MAIL DATE	DELIVERY MODE
04/20/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Advisory Action Before the Filing of an Appeal Brief	Application No.	Applicant(s)	
	10/619,144	CHEN, APHRODITE	
	Examiner	Art Unit	
	RAJ JAIN	2416	

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED 31 March 2009 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE.

1. ☒ The reply was filed after a final rejection, but prior to or on the same day as filing a Notice of Appeal. To avoid abandonment of this application, applicant must timely file one of the following replies: (1) an amendment, affidavit, or other evidence, which places the application in condition for allowance; (2) a Notice of Appeal (with appeal fee) in compliance with 37 CFR 41.31; or (3) a Request for Continued Examination (RCE) in compliance with 37 CFR 1.114. The reply must be filed within one of the following time periods:

a) ☒ The period for reply expires 3 months from the mailing date of the final rejection.

b) ☐ The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection.

Examiner Note: If box 1 is checked, check either box (a) or (b). ONLY CHECK BOX (b) WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

NOTICE OF APPEAL

2. ☐ The Notice of Appeal was filed on _____. A brief in compliance with 37 CFR 41.37 must be filed within two months of the date of filing the Notice of Appeal (37 CFR 41.37(a)), or any extension thereof (37 CFR 41.37(e)), to avoid dismissal of the appeal. Since a Notice of Appeal has been filed, any reply must be filed within the time period set forth in 37 CFR 41.37(a).

AMENDMENTS

3. ☐ The proposed amendment(s) filed after a final rejection, but prior to the date of filing a brief, will not be entered because
   (a) ☐ They raise new issues that would require further consideration and/or search (see NOTE below);
   (b) ☐ They raise the issue of new matter (see NOTE below);
   (c) ☐ They are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or
   (d) ☐ They present additional claims without canceling a corresponding number of finally rejected claims.

   NOTE: _____. (See 37 CFR 1.116 and 41.33(a)).

4. ☐ The amendments are not in compliance with 37 CFR 1.121. See attached Notice of Non-Compliant Amendment (PTOL-324).

5. ☐ Applicant's reply has overcome the following rejection(s): _____.

6. ☐ Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).

7. ☐ For purposes of appeal, the proposed amendment(s): a) ☐ will not be entered, or b) ☐ will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.
   The status of the claim(s) is (or will be) as follows:
   Claim(s) allowed: _____.
   Claim(s) objected to: _____.
   Claim(s) rejected: _____.
   Claim(s) withdrawn from consideration: _____.

AFFIDAVIT OR OTHER EVIDENCE

8. ☐ The affidavit or other evidence filed after a final action, but before or on the date of filing a Notice of Appeal will not be entered because applicant failed to provide a showing of good and sufficient reasons why the affidavit or other evidence is necessary and was not earlier presented. See 37 CFR 1.116(e).

9. ☐ The affidavit or other evidence filed after the date of filing a Notice of Appeal, but prior to the date of filing a brief, will not be entered because the affidavit or other evidence failed to overcome all rejections under appeal and/or appellant fails to provide a showing a good and sufficient reasons why it is necessary and was not earlier presented. See 37 CFR 41.33(d)(1).

10. ☐ The affidavit or other evidence is entered. An explanation of the status of the claims after entry is below or attached.

REQUEST FOR RECONSIDERATION/OTHER

11. ☒ The request for reconsideration has been considered but does NOT place the application in condition for allowance because: See below.

12. ☐ Note the attached Information *Disclosure Statement*(s). (PTO/SB/08) Paper No(s). _____

13. ☐ Other: _____.

/RAJ JAIN/
Examiner, Art Unit 2416

Applicant contends "The address resolution unit 10 (Fig. 1) of Alexander is used to perform an address look-up process, and never performs the learning function" on page 8 of the remarks, however on page 9 the applicant states here in part "...the learning function of Alexander also differs from the packet source address learning process...." Examiner fails to understand Applicant's contention, Applicant is contradicting itself per the remarks on page 9.
Nonetheless, Examiner disagrees, Alexander discloses a multiple port single chip Ethernet switch (Fig. 1, with multiple incoming/outgoing ports) comprising at least the following component parts: a physical layer entity (PHY) including a plurality of ports (Fig. 1, with multiple incoming/outgoing ports); an address table 12 for being written to and read out information to operate the plurality of ports (col 4 lines 21-26); and an address resolution control logic 10 (col 4 lines 39-44, an address learning is invoked via the address resolution unit 10 to incorporate new addresses not in the table 12). The address table creation (learning function) (emphasis added) firmware routing 16 is invoked when an address is not in the address look-up table 12. The packet forwarding firmware 14 or the forwarding logic in conjunction with 12 & 16 performs the learning and forwarding routines.

Applicant further contends Tursich fails to disclose a daisy chain test mode and further contends Tursich fails to disclose "a switch for switching the Ethernet switch to a daisy chain test mode".
Examiner respectfully disagrees, Tursich discloses a daisy chain test mode (Fig. 1, col 1 line 65- col 2 lines 5). Daisy chain test sequence allows for a cost-effective test system that controls the traffic in a daisy-chain of protocol analyzers. The system is implemented with simple control processing that does not add significant cost or complexity to the packet network or to the protocol analyzers. Alexander clearly dislcoses an Ethernet switch (title, col 1 lines 14-40; col 3 lines 1-6). Thus it would have been obvious at the time the invention was made to incorporate the teachings of Tursich within Alexander so as to allow for a cost-effective test system that controls the traffic in a daisy-chain of protocol analyzers.
With regards to a start and stop test ports on a chip, Fig. 1 of Alexander illustrates a single chip implmentation as well as in Tursich (Fig. 2) having a system 100 with plurality of incoming and outgoing ports, one skilled in the art will appreciate the ports of the components are generally fabricated on an integrated chip, thus inherently the test sequence is performed on a chip. Applicant further contends that "... the test packets are transferred between different devices to control testing rather than between the plurality of ports in a single device to test the single device." First off this contention is moot as claims don't expressely require and/or state that it has to be a single device, second (Fig. 2) in Turscich while shows plurality of devices within a system for illustratatvie purposes, the system may also comprise of a single device only further comprising all the components on a single chip as well and therefore satisfying Applicant's contention as well.
Thus based on the foregoing reasoning, Examiner asserts that Alexander (USP 6,553,029 B1) in view of Tursich (USP 6,671,828 B1) does disclose all the limitations of claims 1-14 and therefore the rejection is sustained.